

IDS filed on 02/17/04

D.P. 10/28/04

Page 1 of 1

FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.
SP015.C18 (1397.028000I)

APPLICATION NO.
10/700,520

FIRST NAMED INVENTOR: NGUYEN et al.

FILING DATE
November 5, 2003

ART UNIT
2183

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
AA8						
AB8						
AC8						
AD8						
AE8						
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AH8						
AI8						
AJ8						
AK8						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
AL7						Yes No
AM7						Yes No
AN7						Yes No
AO7						Yes No
AP7						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	31	
<i>dd</i>	AS	31	English language translation of Japanese Application No. 2-130635, dated May 18, 1990, 19 pages.
	AT	31	

EXAMINER

✓ DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

<p style="text-align: center;">O P E INFORMATION DISCLOSURE STATEMENT JAN 09 2004</p>		ATTY. DOCKET NO: SP015.C18 (1397.0280001)		APPLICATION NO.: 10/700,520	
		FIRST NAMED INVENTOR: NGUYEN et al.			
		FILING DATE: November 5, 2003		ART UNIT: To Be Assigned	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA28					
	AB28					
	AC28					
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	AF28					
	AG28					
	AH28					
	AI28					
	AJ28					
	AK28					

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL5					Yes No
AN	AM5	2000-353090A	12/19/2000	Japan		X Yes No
AN	AN5	2000-339159A	12/08/2000	Japan		X Yes No
AN	AO5	2000-339160A	12/08/2000	Japan		X Yes No
	AP5	2000-357091A	12/26/2000	Japan		X Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	28	
AN	AS	28	Notice of Grounds For Rejection, dated October 2, 2003, for Japanese Patent Application No. 2000-145123 (2 pages) with English translation (2 pages).
AN	AT	28	Notice of Grounds For Rejection, dated October 2, 2003, for Japanese Patent Application No. 2000-145124 (2 pages) with English translation (2 pages).

EXAMINER

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT <i>JAN 09 2004</i> <i>JCA</i>	ATTY. DOCKET NO: SP015.C18 (1397.0280001)		APPLICATION NO.: 10/700,520	
	FIRST NAMED INVENTOR: NGUYEN et al.			
	FILING DATE: November 5, 2003		ART UNIT: To Be Assigned	

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL	TRADEMARK	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
		AA29					
		AB29					
		AC29					
		AD29					
		AE29					
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		AI29					
		AJ29					
		AK29					

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
		AL29					Yes
		AM29					No
		AN29					Yes
		AO29					No
		AP29					Yes

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
<i>CD</i>	AR	<u>29</u>	Notice of Grounds for Rejection, dated October 3, 2003, for Japanese Patent Application No. 2000-145125 (3 pages) with English translation (4 pages).				
<i>CD</i>	AS	<u>29</u>	Notice of Grounds for Rejection, dated October 3, 2003, for Japanese Patent Application No. 2000-145126 (3 pages) with English translation (4 pages)				
	AT	<u>29</u>					

EXAMINER	<i>CD</i>			DATE CONSIDERED
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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT				ATTY. DOCKET NO. SP015.C18 (1397.028000I)	APPLICATION NO. 10/700,520		
				FIRST NAMED INVENTOR: NGUYEN et al.			
				FILING DATE November 5, 2003	ART UNIT <i>To Be Assigned</i>		
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
<i>OTTE</i> <i>W</i>	AA7	4,644,466	02/17/1987	Saito			
	AB7						
	AC7						
	AD7						
	AE7						
	AF7						
	AG7						
	AH7						
	AI7						
	AJ7						
	AK7						
FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
<i>CD</i>	AL6	2-130635	05/18/1990	Japan			<input checked="" type="checkbox"/> Yes
<i>W</i>	AM6	0 331 191	09/06/1989	EP			<input type="checkbox"/> No
<i>W</i>	AN6	0 155 211	09/18/1985	EP			<input checked="" type="checkbox"/> Yes
	AO6						<input type="checkbox"/> No
	AP6						<input checked="" type="checkbox"/> Yes
							<input type="checkbox"/> No
OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
<i>W</i>	AR	<u>30</u>	European Search Report issued December 9, 2003 in EP application no. 03 02 4585, 3 pages.				
<i>W</i>	AS	<u>30</u>	Notice of Reason of Rejection, mailed October 24, 2003, for Japanese Appln. No. 2000-146441, 2 pages, accompanied by translation of 2 pages.				
<i>W</i>	AT	<u>30</u>	Notice of Reason of Rejection, mailed October 24, 2003, for Japanese Appln. No. 2000-146442, 2 pages, accompanied by translation of 4 pages.				
EXAMINER				DATE CONSIDERED			
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.							

FORM PTO-1449 <u>INFORMATION DISCLOSURE STATEMENT</u>		ATTY. DOCKET NO. SP015.C18 (1397.028000I)	APPLICATION NO. 10/700,520
		FIRST NAMED INVENTOR: NGUYEN et al.	
		FILING DATE November 5, 2003	ART UNIT To Be Assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
AA8						
AB8						
AC8						
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AG8						
AH8						
AI8						
AJ8						
AK8						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
AL7						Yes
AM7						No
AN7						Yes
AO7						No
AP7						Yes
						No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

<i>A</i>	AR	<u>31</u>	Notice of Reason of Rejection, mailed October 24, 2003, for Japanese Appln. No. 2000-146443, 2 pages, accompanied by translation of 4 pages.
	AS	<u>31</u>	
	AT	<u>31</u>	

EXAMINER

DATE CONSIDERED

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FORM PTO-1449

Fourth Supplemental
INFORMATION DISCLOSURE STATEMENTATTY. DOCKET NO.
SP015.C18 (1397.0280001)APPLICATION NO.
10/700,520

FIRST NAMED INVENTOR: NGUYEN et al.

FILING DATE
November 5, 2003ART UNIT
2183

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
W	AA8	4,901,233	02/13/1990	Liptay			
	AB8	5,134,561	07/28/1992	Liptay			
MAR 2 2004	AC8	5,473,764	12/05/1995	Chi			
	AD8						
	AE8						
	AF8						
	AG8						
	AH8						
	AI8						
	AJ8						
	AK8						

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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
W	AL7	64 36336	02/07/1989	Japan			Yes
	AM7						No
	AN7						Yes
	AO7						No
	AP7						Yes
							No

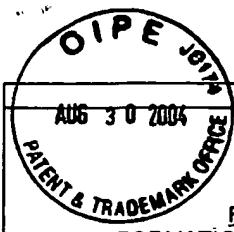
OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	31	
	AS	31	
W	AT	31	Final Rejection, mailed January 30, 2004, for Japanese Appl. No. 2000-146443, and English language translation of same, 3 pages.

EXAMINER

DATE CONSIDERED

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FORM PTO-1449 Fifth Supplemental INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. SP015.C18 (1397.0280001)	APPLICATION NO. 10/700,520
	FIRST NAMED INVENTOR: NGUYEN et al.	
	FILING DATE November 5, 2003	ART UNIT 2183

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
AA8						
AB8						
AC8						
AD8	4,833,599	05/23/1989	Colwell et al.			
AE8	4,974,154	11/27/1990	Matsuo			
AF8	5,142,634	08/25/1992	Fite et al.			
AG8						
AH8						
AI8						
AJ8						
AK8						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
AL7						Yes
AM7	HEI2-130635	05/18/1990	JAPAN	—	—	No
AN7						Yes
AO7						No
AP7						Yes

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

AR	32	Findlay, et al., "HARP: A VLIW RISC Processor", Proceeding of 5 th Annual European Computer Conference on Advanced Computer Technology, Reliable Systems and Applications, May 16, 1991, pp. 368-372.
AS	32	Kuga et al., "DSNS (Dynamically-hazard-resolved, Statically-code-scheduled, Nonuniform Superscalar): Yet Another Superscalar Processor Architecture", Dept. of Information Systems, Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, Fukuoka, Japan, pp. 14-29.
AT	32	Colwell et al., "A VLIW Architecture For A Trace Scheduling Compiler", Association For Computing Machinery (ACM), 1987, pp. 180-192.

EXAMINER	<i>W. X. Z.</i>	DATE CONSIDERED <i>10/28/04</i>
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FORM PTO-1449 <u>INFORMATION DISCLOSURE STATEMENT</u>		ATTY. DOCKET NO. SP015.C18	APPLICATION NO. To Be Assigned
		APPLICANT Nguyen et al.	
		FILING DATE Herewith	GROUP To be assigned

U. S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
W	AA1	3,346,851	10/1967	Thornton et al.			
W	AB1	3,718,912	02/1973	Hasbrouck et al.			
W	AC1	3,771,138	11/1973	Celtruda et al.			
W	AD1	3,789,365	01/1974	Jen et al.			
W	AE1	4,034,349	07/1977	Monaco et al.			
W	AF1	4,200,927	04/1980	Hughes et al.			
W	AG1	4,228,495	10/1980	Bernhard et al.			
W	AH1	4,296,470	10/1981	Fairchild et al.			
W	AI1	4,315,314	02/1982	Russo			
W	AJ1	4,410,939	10/1983	Kawakami			
W	AK1	4,434,461	02/1984	Puhl			

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
W	AL1	0 479 390 A2	08/1992	EP			Yes No
W	AM1	0 426 393	08/1991	EP			Yes No
W	AN1	0 419 105 A2	10/1990	EP			Yes No
W	AO1	0 402 856	12/1990	EP			Yes No
W	AP1	0 377 991 A3	12/1989	EP			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
W	AR	1	8-Bit Embedded controller Handbook, Intel, 1989, pp. 1-1- 1-19 and 3-1 -3-37.				
W	AS	1	Acosta, Raymond D. et al., "An Instruction Issuing Approach to Enhancing Performance in Multiple Functional Unit Processors," IEEE Transactions on Computers, Vol. C-35, No. 9, September 1986, pp. 815-828.				
W	AT	1	Agerwala et al., "High Performance Reduced Instruction Set Processors," IBM Research Division, March 31, 1987, pp. 1-61.				

EXAMINER	<i>W</i>	DATE CONSIDERED
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		FILING DATE Herewith	GROUP To be assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
W	AA2	4,459,657	07/1984	Murao			
W	AB2	4,476,525	10/1984	Ishii			
W	AC2	4,626,989	12/1986	Torii			
W	AD2	4,675,806	06/1987	Uchida			
W	AE2	4,714,994	12/1987	Oklobdzija et al.			
W	AF2	4,722,049	01/1988	Lahti			
W	AG2	4,752,873	06/1988	Shonai et al.			
W	AH2	4,758,948	07/1988	May et al.			
W	AI2	4,766,566	08/1988	Chuang			
W	AJ2	4,807,115	02/1989	Torng			
W	AK2	4,858,105	08/1989	Kuriyama et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
W	AL2	0 372 751 A2	11/1989	EP			Yes No
W	AM2	0 368 332 A2	05/1990	EP			Yes No
W	AN2	0 354 585 A2	02/1990	EP			Yes No
W	AO2	0 171 595 A2	02/1986	EP			Yes No
W	AP2	0 136 179 A2	09/1984	EP			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

W	AR	2	Aiken, A. and Nicolau, A., "Perfect Pipelining: A New Loop Parallelization Technique*," pp. 221-235.
W	AS	2	Andrews, Distinctions Blur Between DSP Solutions, Computer Design, Vol. 28, No. 9, May 1, 1989, Littleton, Mass., pp. 86-99.
W	AT	2	Charlesworth, A.E., "An Approach to Scientific Array Processing: The Architectural Design of the AP-120B/FPS-164 Family," Computer, Vol. 14, September 1981, pp. 18-27.

EXAMINER

DATE CONSIDERED

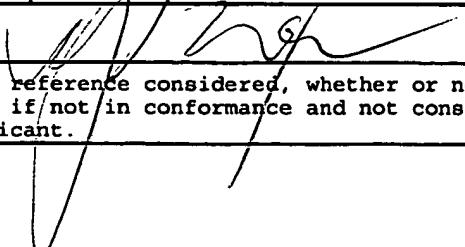
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U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA3	4,897,810	01/1990	Nix			
	AB3	4,901,228	02/1990	Kodama			
	AC3	4,901,233	02/1990	Liptay			
	AD3	4,903,196	02/1990	Pomerene et al.			
	AE3	4,924,376	05/1990	Ooi			
	AF3	4,926,323	05/1990	Baror et al.			
	AG3	4,942,525	07/1990	Shintani et al.			
	AH3	4,985,825	01/1991	Webb, Jr. et al.			
	AI3	4,992,938	02/1991	Cocke et al.			
	AJ3	5,003,462	03/1991	Blaner et al.			
	AK3	5,101,341	03/1992	Circella et al.			

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL3	2 575 564	12/1985	FR			Yes No
	AM3	2 011 682	11/1979	GB			Yes No
	AN3	61-95447	06/1986	JP			Yes No
	AO3	2-278337	11/1990	JP			Yes No
	AP3	3-137729	06/1991	JP			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
	AR	3	Colwell et al., "A VLIW Architecture for a Trace Scheduling Compiler," Proceedings of the 2 nd International Conference on Architectural Support for Programming Languages and Operating Systems, October 1987, pp. 180-192.				
	AS	3	Foster et al., "Percolation of Code to Enhance Parallel Dispatching and Execution," IEEE Trans. On Computers, December 1971, pp. 1411-1415.				
	AT	3	Goodman, J.R. and Hsu, W., "Code Scheduling and Register Allocation in Large Basic Blocks," ACM, 1988, pp. 442-452.				

EXAMINER		DATE CONSIDERED
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		FILING DATE Herewith	GROUP To be assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
W	AA4	5,127,091	02/1995	Horst			
W	AB4	5,129,067	07/1992	Johnson			
W	AC4	5,134,561	07/1992	Liptay			
W	AD4	5,155,843	10/1992	Stamm et al.			
W	AE4	5,187,796	02/1993	Wang et al.			
W	AF4	5,226,126	07/1993	McFarland et al.			
W	AG4	5,226,170	07/1993	Rubinfeld			
W	AH4	5,230,068	07/1993	Van Dyke et al.			
W	AI4	5,355,460	10/1994	Eickenmeyer et al.			
W	AJ4	5,442,757	08/1995	McFarland et al.			
W	AK4	5,461,715	10/1995	Matsuo et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
W	AL4	3-147134	06/1991	JP			Yes No
W	AM4	2-22736	01/1990	JP			Yes No
W	AN4	2-87229	03/1990	JP			Yes No
W	AO4	3-35322	02/1991	JP			Yes No
W	AP4	64-36366	02/1989	JP			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

W	AR	4	Gross et al., "Optimizing Delayed Branches," Proceedings of the 5 th Annual Workshop on Microprogramming, October 5-7, 1982, pp. 114-120.
W	AS	4	Groves, R.D. and Oehler, R., "An IBM Second Generation RISC Processor Architecture," IEEE, 1989, pp. 134-137.
W	AT	4	Bakoglu et al., "IBM Second-Generation RISC Machine Organization," 1990, IEEE, pp. 173-178.

EXAMINER *W* DATE CONSIDERED *8/3/95*

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT		ATTY. DOCKET NO. SP015.C18	APPLICATION NO. To Be Assigned
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U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
<i>SL</i>	AA5	5,487,156	01/1996	Popescu et al.			
<i>SL</i>	AB5	5,488,729	01/1996	Vesegna et al.			
<i>SL</i>	AC5	5,539,911	07/1996	Nguyen et al.			
<i>SL</i>	AD5	5,561,776	10/1996	Popescu et al.			
<i>SL</i>	AE5	5,574,927	11/1996	Scantlin			
<i>SP</i>	AF5	5,592,636	01/1997	Popescu et al.			
<i>SL</i>	AG5	5,625,837	04/1997	Popescu et al.			
<i>SL</i>	AH5	5,627,983	05/1997	Popescu et al.			
<i>SL</i>	AI5	5,651,125	07/1997	Witt et al.			
<i>SL</i>	AJ5	5,689,720	11/1997	Nguyen et al.			
<i>SL</i>	AK5	5,708,841	01/1998	Popescu et al.			

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
<i>SL</i>	AL5	2-130634	05/1990	Japan			Yes No
	AM5						Yes No
	AN5						Yes No
	AOS						Yes No
	AP5						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
<i>SL</i>	AR	5	H. Nakano et al., "A 80 Mflops 64-bit Microprocessor for Parallel Computer," 1991, IEEE, pp. 15.2.1-15.2.4.				
<i>SL</i>	AS	5	Hennessy et al., Computer Architecture: A Quantitative Approach, Morgan Kaufman Publishers, Inc., 1990 (in its entirety).				
<i>SL</i>	AT	5	Horst, R.W. et al., "Multiple Instruction Issue in the NonStop Cyclone Processor," IEEE, 1990, pp. 216-226.				

EXAMINER	<i>SL</i>	DATE CONSIDERED
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		FILING DATE Herewith	GROUP To be assigned	

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
W	AA6	5,768,575	06/1998	McFarland et al.			
W	AB6	5,778,210	07/1998	Henstrom et al.			
W	AC6	5,797,025	08/1998	Popescu et al.			
W	AD6	5,832,205	11/1998	Kelly et al.			
W	AE6	5,832,293	11/1998	Popescu et al.			
W	AF6	5,961,629	10/1999	Nguyen et al.			
W	AG6	6,038,654	03/2000	Nguyen et al.			
W	AH6	6,092,181	07/2000	Nguyen et al.			
W	AI6	6,101,594	08/2000	Nguyen et al.			
W	AJ6	6,128,723	10/2000	Nguyen et al.			
W	AK6	5,233,694	08/1993	Hotta et al.			

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL6						Yes No
	AM6						Yes No
	AN6						Yes No
	AO6						Yes No
	AP6						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
W	AR	6	Hwu et al., "HPSm, a High Performance Restricted Data Flow Architecture Having Minimal Functionality," Proceedings from ISCA-13, Tokyo, Japan, June 2-5, 1986, pp. 297-306.				
W	AS	6	Hwu et al., "Checkpoint Repair for High-Performance Out-of-Order Execution Machines," IEEE Trans. On Computers, Vol. C-36, NO. 12, December 1987, pp. 1496-1514.				
W	AT	6	Hwu et al., "Exploiting Parallel Microprocessor Microarchitectures with a Compiler Code Generator," Proceedings of the 15 th Annual Symposium on Computer Architecture, June 1988, pp. 45-53.				

EXAMINER	DATE CONSIDERED
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.	

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT		ATTY. DOCKET NO. SP015.C18	APPLICATION NO. To Be Assigned
		APPLICANT Nguyen et al.	
		FILING DATE Herewith	GROUP To be assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
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OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

60	AR	7	IBM Journal of Research and Development, Vol. 34, No. 1, January 1990, pp. 1-70.
60	AS	7	IBM Technical Disclosure Bulletin, Overlap of Store Multiple Operation With Succeeding Operations through Second Set of General Purpose Registers, Vol. 28, No. 6, November 1989, New York, NY, pp. 2727-2728.
60	AT	7	Jelemensky, New Microcomputer Features Advanced Hardware For Real-Time Control Applications, Electro Conference Record, Vol. 14, April 11, 1989, Los Angeles, CA, pp. 511-519.

EXAMINER

DATE CONSIDERED

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	AM8						Yes No
	AN8						Yes No
	AO8						Yes No
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OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
<i>W</i>	AR	8	Johnson, William M., Super-Scalar Processor Design, (Dissertation), copyright 1989, 134 pages.				
<i>W</i>	AS	8	Johnson, William M., Super-Scalar Processor Design, Prentice-Hall, Inc., 1991 (in its entirety).				
<i>W</i>	AT	8	Jouppi, N.H., "Integration and Packaging Plateaus of Processor Performance," IEEE, 1989, pp. 229-232.				
EXAMINER <i>W</i>					DATE CONSIDERED <i>W</i>		

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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		APPLICANT Nguyen et al.	
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OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
	AR	9	Jouppi, N.P., "The Nonuniform Distribution of Instruction-Level and Machine Parallelism and Its Effect on Performance," IEEE Transactions on Computers, Vol. 38, No. 12, December 1989, pp. 1645-1658.				
	AS	9	Jouppi et al., "Available Instruction-Level Parallelism for Superscalar and Superpipelined Machines," Proceedings of the 3rd International Conference on Architectural Support for Programming Languages and Operating Systems, April 1989, pp. 272-282.				
	AT	9	Keller, R.M., "Look-Ahead Processors," Computing Surveys, Vol. 7, No. 4, December 1975, pp. 177-195.				

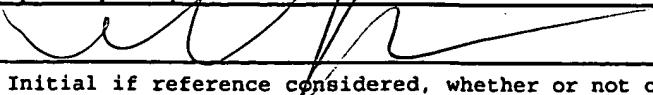
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	AO10						Yes No
	AP10						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
	AR	<u>10</u>	Lam, M.S., "Instruction Scheduling For Superscalar Architectures," Annu. Rev. Comput. Sci., Vol. 4, 1990, pp. 173-201.				
	AS	<u>10</u>	Lee, Ruby B., "Precision Architecture," COMPUTER, January 1989, pp. 78-91.				
	AT	<u>10</u>	Melear, C., Motorola, Inc., The Design of the 88000 RISC Family, IEEE MICRO, Vol. 9, No. 2, April 1989, Los Alamitos, CA, pp. 26-38.				

EXAMINER		DATE CONSIDERED
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	AO11						Yes No
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OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	<u>11</u>	Murakami, K. et al., "SIMP (Single Instruction Stream/Multiple Instruction Pipelining): A Novel High-Speed Single-Processor Architecture," ACM, 1989, pp. 78-85.
	AS	<u>11</u>	Odnert, D. et al., "Architecture and Compiler Enhancements for PA-RISC Workstations," Proceedings from IEEE Compcon, February 25-March 1, 1991, San Francisco, CA, pp. 214-218.
	AT	<u>11</u>	Patent Abstracts of Japan, Vol. 010, No. 089, April 1986, & JP, A, 60 225 943 (Hitachi Seisakusho K K) November 11, 1985.

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DATE CONSIDERED

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	AO12						Yes No
	AP12						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
<i>JP</i>	AR	<u>12</u>	Patt et al., "Critical Issues Regarding HPS, A High Performance Microarchitecture," Proceedings of the 18 th Annual Workshop on Microprogramming, December 1985, pp. 109-116.				
<i>JP</i>	AS	<u>12</u>	Patt et al., "HPS, A New Microarchitecture: Rationale and Introduction," Proceedings of the 18 th Annual Workshop on Microprogramming, December 1985, pp. 103-108.				
<i>AT</i>	AT	<u>12</u>	Pleszkun et al., "The Performance Potential of Multiple Functional Unit Processors," Proceedings of the 15 th Annual Symposium on Computer Architecture, June 1988, pp. 37-44.				

EXAMINER	<i>JP</i>	DATE CONSIDERED
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.		

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		APPLICANT Nguyen et al.		
		FILING DATE Herewith	GROUP To be assigned	

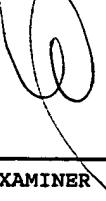
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	AO13					Yes No
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OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	<u>13</u>	Pleszkun et al., "WISQ: A Restartable Architecture Using Queues," Proceedings of the 14 th International Symposium on Computer Architecture, June 1987, pp. 290-299.
	AS	<u>13</u>	Popescu et al., The Metaflow Architecture, Metaflow Technologies, Inc., June 1991(in its entirety).
	AT	<u>13</u>	S. McGeady, "The i960A Superscalar Implementation of the 80960 Architecture," IEEE, 1990, pp. 232-240.

EXAMINER	DATE CONSIDERED
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	AL14						Yes No
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	AN14						Yes No
	AO14						Yes No
	AP14						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
	AR	<u>14</u>	Smith et al., Implementation Precise Interrupts in Pipelined Processors, IEEE Transactions on Computers, Vol. 37, No. 5, May 1988, New York, NY, p. 562, 573.				
	AS	<u>14</u>	Smith et al., "Implementation of Precise Interrupts in Pipelined Process," Proceedings of the 12 th Annual International Symposium on Computer Architecture, June 1985, pp. 36-44.				
	AT	<u>14</u>	Smith et al., "Limits on Multiple Instruction Issue," Proceedings of the 3 rd International Conference on Architectural Support for Programming Languages and Operating Systems, April 1989, pp. 290-302.				
EXAMINER					DATE CONSIDERED		

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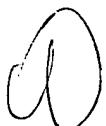
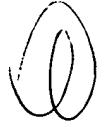
OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
	AR	<u>15</u>	Smith, M.D. et al., "Boosting Beyond Static Scheduling in a Superscalar Processor," IEEE, 1990, pp. 344-354.				
	AS	<u>15</u>	Sohi, Gurindar S. and Sriram Vajapeyam, "Instruction Issue Logic for High-Performance, Interruptable Pipelined Processors," Conference Proceedings of the 14 th Annual International Symposium on Computer Architecture, June 2-5, 1987, pp. 27-34.				
	AT	<u>15</u>	Thornton, J.E., Design of a Computer: The Control Data 6600, Control Data Corporation, 1970, pp. 58-140.				

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	AO16						Yes No
	AP16						Yes No

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	AR	16	Tjaden et al., "Detection and Parallel Execution of Independent Instructions," IEEE Trans. On Computers, Vol. C-19, No. 10, October 1970, pp. 889-895.				
	AS	16	Tjaden et al., "Representation of Concurrency with Ordering Matrices," IEEE Trans. On Computers, Vol. C-22, No. 8, August 1973, pp. 752-761.				
	AT	16	Tjaden, Representation and Detection of Concurrency Using Ordering Matrices, (Dissertation) 1972, pp. 1-199.				

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OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
<i>W</i>	AR	<u>17</u>	Tomasulo, R.M., "An Efficient Algorithm for Exploiting Multiple Arithmetic Units," IBM Journal, Vol. 11, January 1967, pp. 25-33.				
<i>O</i>	AS	<u>17</u>	Uht, A.K., "An Efficient Hardware Algorithm to Extract Concurrency From General-Purpose Code," Proceedings of the 19 th Annual Hawaii International Conference on System Sciences, 1986, pp. 41-50.				
<i>W</i>	AT	<u>17</u>	Wedig, R.G., Detection of Concurrency in Directly Executed Language Instruction Streams, (Dissertation), June 1982, pp. 1-179.				
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		AP18					Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
	AR	<u>18</u>	Weiss, R., Third-Generation RISC Processors, On Special Report, March 30, 1992, pp. 96-108.				
	AS	<u>18</u>	Weiss et al., "Instruction Issue Logic in Pipelined Supercomputers," Reprinted from IEEE Trans. On Computers, Vol. C-33, No. 11, November 1984, pp. 1013-1022.				
	AT	<u>18</u>	English Language Translation of Japanese Patent Appl. No. 61-95447, published May 14, 1986, 15 pages.				
EXAMINER					DATE CONSIDERED		

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		APPLICANT Nguyen et al.	
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U.S. PATENT DOCUMENTS

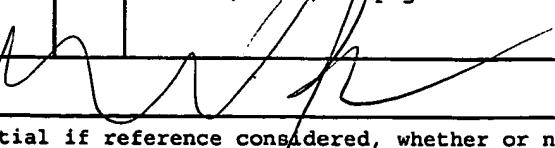
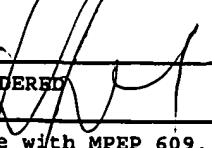
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	AO19						Yes No
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OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	<u>19</u>	English Language Translation of Japanese Patent Appl. No. 2-278337, published November 14, 1990, 20 pages.
	AS	<u>19</u>	English Language Translation of Japanese Patent Appl. No. 3-137729, published June 12, 1991, 7 pages.
	AT	<u>19</u>	English Language Translation of Japanese Patent Appl. No. 3-147134, published June 24, 1991, 18 pages.

EXAMINER  DATE CONSIDERED 

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U. S. PATENT DOCUMENTS

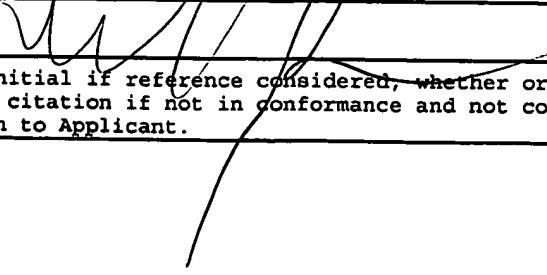
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OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	20	Kuga Morio et al., "Performance Evaluation of the Superscalar Processor "SIMP" based on the SIMP (Single Instruction Stream/Multiple Instruction Pipeline) Architecture," Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, 1990, pp. 337-344.
	AS	20	English Language Translation, Kuga Morio et al., "Performance Evaluation of the Superscalar Processor "SIMP" based on the SIMP (Single Instruction Stream/Multiple Instruction Pipeline) Architecture," Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, 1990, pp. 337-344, (Document AR20).
	AT	20	Kuga Morihiro et al., "Low-Level Parallel Processing Algorithm for the SIMP Processor Prototype," Department of Information Systems, Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, Vol. 30, No. 12, Dec. 1989, pp. 1603-1611.

EXAMINER		DATE CONSIDERED
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL21						Yes No
	AM21						Yes No
	AN21						Yes No
	AO21						Yes No
	AP21						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

<i>Q</i>	AR	<u>21</u>	English Language Translation, Kuga Morihiro et al., "Low-Level Parallel Processing Algorithm for the SIMD Processor Prototype," Department of Information Systems, Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, Vol. 30, No. 12, Dec. 1989, pp. 1603-1611, (Document AT20).
<i>W</i>	AS	<u>21</u>	US Application 09/336,589, Senter Cheryl et al., June 21, 1999.
<i>W</i>	AT	<u>21</u>	Colwell et al., "A VLIW Architecture for a Trace Scheduling Compiler," Proceedings of the 2 nd International Conference on Architectural Support for Programming Languages and Operating Systems, October 5-8, 1987, California.

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT		ATTY. DOCKET NO. SP015.C18	APPLICATION NO. To Be Assigned	
		APPLICANT Nguyen et al.		
		FILING DATE Herewith	GROUP To be assigned	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
AA22						
AB22						
AC22						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
AL22						Yes No
AM22						Yes No
AN22						Yes No
AO22						Yes No
AP22						

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

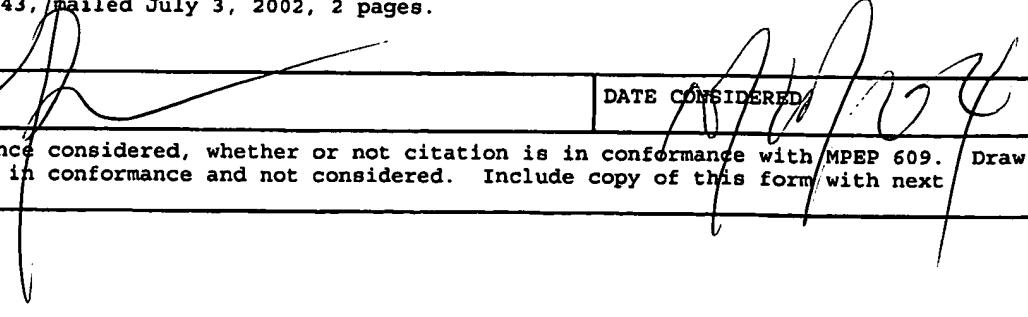
<i>W</i>	AR	<u>22</u>	Notification of Reason for Refusal for Japanese Patent Application No. 2000-145123, mailed June 26, 2002, 2 pages.
<i>W</i>	AS	<u>22</u>	Notification of Reason for Refusal for Japanese Patent Application No. 2000-145124, mailed June 26, 2002, 2 pages.
<i>J</i>	AT	<u>22</u>	Notification of Reason for Refusal for Japanese Patent Application No. 2000-145125, mailed June 26, 2002, 2 pages.

EXAMINER	<i>Weld</i>	DATE CONSIDERED
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.		

FORM PTO-1449 <u>INFORMATION DISCLOSURE STATEMENT</u>		ATTY. DOCKET NO. SP015.C18	APPLICATION NO. To Be Assigned
		APPLICANT Nguyen et al.	
		FILING DATE Herewith	GROUP To be assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
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		AI23					
		AJ23					
		AK23					

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
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		AO23					Yes No
		AP23					Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
	AR	23	Notification of Reason for Refusal for Japanese Patent Application No. 2000-145126, mailed July 3, 2002, 2 pages.				
	AS	23	Notification of Reason for Refusal for Japanese Patent Application No. 2000-146442, mailed July 3, 2002, 2 pages.				
	AT	23	Notification of Reason for Refusal for Japanese Patent Application No. 2000-146443, mailed July 3, 2002, 2 pages.				
EXAMINER				DATE CONSIDERED 			

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		APPLICANT Nguyen et al.		
		FILING DATE Herewith	GROUP To be assigned	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA24					
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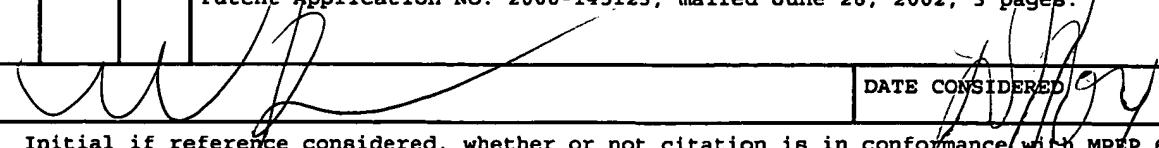
FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
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	AM24					Yes No
	AN24					Yes No
	AO24					Yes No
	AP24					Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	<u>24</u>	English-language translation of Japanese Laid-Open Patent Application No. H02-22736, (January 25, 1990 - date of publication), 10 pages.
	AS	<u>24</u>	English-language translation of Japanese Laid-Open Patent Application No. H02-87229, (March 28, 1990 - date of publication), 5 pages.
	AT	<u>24</u>	English-language translation of Notification of Reason for Refusal for Japanese Patent Application No. 2000-145123, mailed June 26, 2002, 3 pages.

EXAMINER

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	APPLICANT Nguyen et al.	
	FILING DATE Herewith	GROUP To be assigned

U. S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
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	AM25						Yes No
	AN25						Yes No
	AO25						Yes No
	AP25						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

AR	<u>25</u>	English-language translation for Notification of Refusal for Japanese Patent Application No. 2000-145124, mailed June 26, 2002, 3 pages.
AS	<u>25</u>	English-language translation for Notification of Refusal for Japanese Patent Application No. 2000-145125, mailed June 26, 2002, 4 pages.
AT	<u>25</u>	English-language translation for Notification of Refusal for Japanese Patent Application No. 2000-145126, mailed July 3, 2002, 3 pages.
EXAMINER		DATE CONSIDERED
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		APPLICANT Nguyen et al.	
		FILING DATE Herewith	GROUP To be assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
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FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
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	AM26						Yes No
	AN26						Yes No
	AO26						Yes No
	AP26						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
	AR	<u>26</u>	English-language translation for Notification of Reason for Refusal for Japanese Patent Application No. 2000-146442, mailed July 3, 2002, 4 pages.				
	AS	<u>26</u>	English-language translation for Notification of Reason for Refusal for Japanese Patent Application No. 2000-146443, mailed July 3, 2002, 4 pages.				
	AT	<u>26</u>	Kuga Morihiro et al., "Low-Level Parallel Processing Algorithms for the "Shinpu" Processor Based on the SIMD (Single Instruction Stream / Multiple Instruction Pipelining) Method, Department of Information System, Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, Vol. 30, No. 12, December 1989, pages 1603-1611.				
EXAMINER					DATE CONSIDERED		
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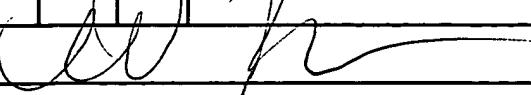
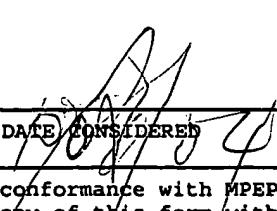
FORM PTO-1449 <u>INFORMATION DISCLOSURE STATEMENT</u>		ATTY. DOCKET NO. SP015.C18	APPLICATION NO. To Be Assigned
		APPLICANT Nguyen et al.	
		FILING DATE Herewith	GROUP To be assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA27						
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FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL27						Yes No
	AM27						Yes No
	AN27						Yes No
	AO27						Yes No
	AP27						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
EXAMINER		DATE	DESCRIPTION				
	AR	27	English-language translation, Kuga Morihiro et al., "Low-Level Parallel Processing Algorithms for the "Shinpu" Processor Based on the SIMD (Single Instruction Stream / Multiple Instruction Pipelining) Method, Department of Information System, Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, Vol. 30, No. 12, December 1989, pages 1603-1624.				
	AS	27	Final Rejection from Japanese Patent Appl. No. 502150, 1 page, (July 16, 2002)				
	AT	27	English translation of Final Rejection from Japanese Patent Appl. No. 502150, 1 page, (July 16, 2002)				
EXAMINER				DATE CONSIDERED			

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			APPLICANT Nguyen et al.				
			FILING DATE Herewith		GROUP To be assigned		
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
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FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL28						Yes No
	AM28						Yes No
	AN28						Yes No
	AO28						Yes No
	AP28						Yes No
OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
		AR	<u>28</u>	English translation of Japanese Laid Open Patent Appl. No. H02-130634, (May 18, 1990 - date of publication), 56 pages.			
		AS	<u>28</u>				
		AT	<u>28</u>				
EXAMINER 				<input type="checkbox"/> DATE CONSIDERED 			
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.							